> array package. (Terui, column 1, lines 13-15, emphasis added.)

They are intended to be mounted on motherboards like applicants' PC wiring boards. Note that applicants' claim 11 recites:

> A thermally enhanced printed circuit (PC) wiring board for ball grid integrated circuit packages....

Further, Terui states:

> With the foregoing in view, it is therefore an object of the present invention to provide a semiconductor device capable of preventing the radiation of an electromagnetic wave to the outside and a malfunction developed due to an electromagnetic wave sent from the outside. (Terui, column 1, 31-35.)

Terui further states:

> ...and a conductive cap for covering the semiconductor element electrically connected to a ground potential. (Column 1, lines 41-42.)

The first two embodiments of Terui shown in Figs. 1 and 4 have only a conductive cap 15. In the embodiment shown in Fig. 5, the difference from the first two embodiments is that it is formed by a:

> ...multilayer board 30 provided therewithin with an intermediate layer 31 formed by a conductive layer. (Terui, column 4, lines 47-51.)

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> Owing to the provision of the intermediate layer 31..., the semiconductor element 12 is electrically cut off from the outside by a metal-made cap and the intermediate layer [31] so that a higher shield effect can be expected. (Terui, column 5, lines 8-12.)

Terui relates to a small-sized area array package and that his objective is to provide a conductive metal shell around the semiconductor element 12. Terui does not teach or suggest a

"thermally enhanced printed circuit (PC) wiring board for ball grid integrated circuit packages." While applicants acknowledge the validity of the principle cited and relied upon by the Examiner and *Ex parte Masham, 2 USPQ 2d 1647 (1987)*, applicants respectfully submit that it is inapplicable in the present case.

Note, for example, that applicants' claim 11 calls for a wiring board for "ball grid integrated circuit packages."

What the Examiner is really doing is relabeling Terui's multilayer board element 30 in an attempt to make it into something which it is not.

The discussion throughout the Terui reference refers to his device as an attachment to a "motherboard" and particularly in connection with the embodiment shown in Fig. 5:

> In a manner similar to the case described in the second embodiment even in the case of the third embodiment, the cap may be provided with the support pins so as to extend through the through holes defined in the corners of the board. In this case, the amount of sinking of the package due to the melting of each external terminal at the mounting of the motherboard can be adjusted so that the package can be prevented from excessively sinking upon mounting of the motherboard. Further, flux cleanability after the mounting of the motherboard and the reliability of connection with the motherboard can be improved. (Terui, column 5, lines 29-30, emphasis added.)

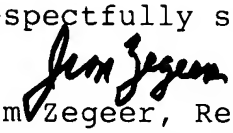
In the present case, applicants' printed wiring board corresponds to Terui's motherboard.

In view of the above, the rejection of claims 11, 12, 15 and 16 under 35 U.S.C. §102(e) is in error.

Reconsideration of the rejection of claims 13, 14 and 17 under 35 U.S.C. §103(a) as being unpatentable over Terui in view of Adlam (US 5,861,076) is respectfully requested. As shown above, Terui relates to small-sized area array packages and does not relate to or disclose in any manner, fashion or form a structure which can be used as a printed circuit wiring board, e.g. a motherboard. Adlam does not change this fact.

In view of the above, further and favorable reconsideration is respectfully requested.

Respectfully submitted,



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In the event this paper is deemed not timely filed, the applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 26-0090